

A GSM-Based Clock-Harvesting Receiver With -87 dBm Sensitivity for Sensor Network Wake-Up

Jonathan K. Brown, *Member, IEEE*, and David D. Wentzloff, *Member, IEEE*

Abstract—This paper presents a new type of wake-up receiver, called a clock-harvesting receiver, which extracts a 21 Hz clock embedded within the GSM standard for the wake-up of a wireless sensor network. The receiver was fabricated in $0.13\ \mu\text{m}$ CMOS and harvests a 21 Hz clock from the 1900-MHz GSM band. It was designed for heavily duty-cycled operation to reduce the energy required for synchronization of a network. In active mode, the receiver achieves a sensitivity of -87 dBm with $57\ \mu\text{s}$ of jitter while consuming $126\ \mu\text{W}$. In sleep mode, the power consumption is $81\ \text{pW}$. Experiments conducted in the lab verify the functionality of the receiver with a real local GSM cellular signal.

Index Terms—Analog integrated circuits, global system for mobile communications (GSM), clock-harvesting receiver (CRX), synchronization, wake-up receiver (WRX), wireless sensor networks (WSNs).

I. INTRODUCTION

WIRELESS sensor networks (WSNs) are perceived as the next big step in a decades-long trend toward smaller, more pervasive computing. For many applications, such as environmental, infrastructure, and health monitoring, long lifetimes are desired from small sensor nodes. As a result, low power consumption is critical.

A typical sensor node consists of five major components: a communication radio, a microprocessor, a battery, a timer, and sensors. Unfortunately, the battery often has insufficient energy to operate a sensor node continuously for its desired lifetime. To alleviate this problem, energy usage must be reduced. The radio and timer easily dominate system energy usage when operated continuously for the purposes of synchronization. Thus, reducing the power consumed to maintain synchronization can greatly improve node lifetime [1]. The traditional (and perhaps obvious) approach to reducing average power consumption is to duty-cycle the communication radio and schedule communication using a high-accuracy on-node timer. Unfortunately, high-accuracy timers require relatively high powers in comparison with less accurate timers. In addition, high-accuracy timers across multiple sensor nodes will eventually drift apart, unlike networks which share a common timing reference.

Manuscript received November 29, 2011; revised January 11, 2013; accepted January 20, 2013. Date of current version February 20, 2013. This paper was approved by Associate Editor Roland Thewes. This material is based upon work supported by the National Science Foundation under Grant No. CNS-1035303.

The authors are with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109 USA (e-mail: jkbrown@umich.edu).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2013.2242716

An alternative approach replaces the accurate on-node timer with an always-on wake-up receiver (WRX) [2], [3]. WRXs allow the nodes in a WSN to operate in a low-power sleep mode and use a wireless signal to wake the nodes up. A traditional WRX remains on continuously during sleep mode, waking-up the node after a signal is broadcast within the WSN (Fig. 1(a)). As a result, a WRX enables fully asynchronous, interrupt-based communication.

To further conserve energy in the WSN, the high-power wake-up beacon should be eliminated from networks with symmetric communication links since the nodes already operate from a constrained power budget. The wake-up receiver can instead harvest a digital clock from an existing wireless standard such as Wi-Fi, broadcast TV, or cellular signals. We call this a clock-harvesting receiver (CRX). This paper presents a CRX designed to extract a 21 Hz clock from a synchronization signal embedded within every broadcast channel (BCH) of the GSM mobile phone standard for the wake-up of a WSN.

The clock-harvesting receiver can be duty-cycled to further reduce synchronization energy as part of a hierarchical synchronization strategy. By coarsely duty-cycling the CRX (with an on-node $<1\ \text{nW}$ program-and-hold timer, for example [4]), the CRX could be fully-powered only momentarily around the 21 Hz GSM clock edges with a timer optimized for this system. During the remaining time the CRX is asleep, so the receiver is designed with a $<100\ \text{pW}$ sleep mode. By aligning each node to the arrival of the next GSM-harvested clock edge, the entire WSN is synchronized and may selectively enable communication radios based on higher-layer network policies (Fig. 1(b)).

While the CRX requires an external local oscillator (LO) to select the desired GSM signal, a fixed-frequency LO should be sufficient for many WSNs. Fortunately, a low-power LO could be generated using an FBAR-based oscillator which consumes $<100\ \mu\text{W}$ and satisfies the requirements of this system [5], [6].

This work presents the entire design of a fully-characterized CRX starting in Section II with a discussion of the requirements for a wake-up source, the operation of the CRX, and the system architecture. In Section III, we describe the simulation results for designing the bandpass filters. The design of each circuit used in the receiver is discussed in Section IV, followed by measurement results in Section V. Finally, we conclude with a demonstration of the CRX by extracting a clock from a local GSM cell signal.

II. SYSTEM OVERVIEW

This section provides an overview of GSM-based synchronization, the system operation of the CRX and its architecture, and intermediate frequency selection.

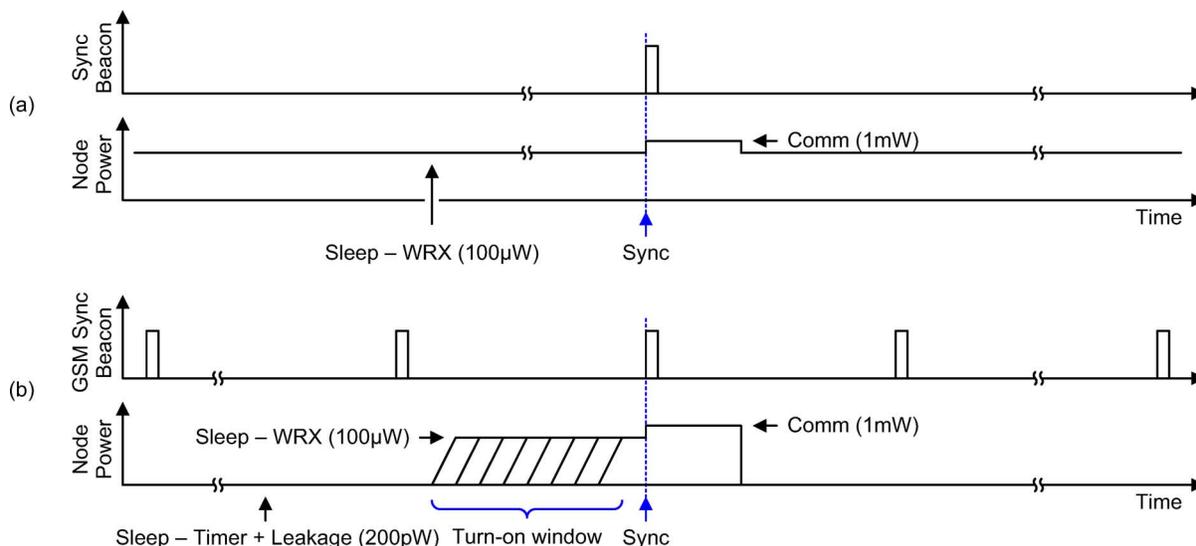


Fig. 1. WSN synchronization (a) with an always-on wake-up receiver and (b) with a duty-cycled wake-up receiver.

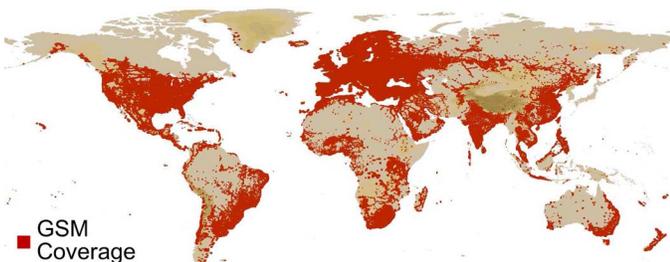


Fig. 2. The 2009 Global System for Mobile Communications (GSM) worldwide coverage map, excluding 3 GSM coverage [7].

A. GSM-Based Synchronization

GSM was selected as a wake-up source because it provides a pervasive and practical signal for use in WSN wake-up. GSM is a global standard (Fig. 2) that covers much of the inhabited world, including North America, Europe, China, and India [7]. Japan is one notable exception. A single GSM broadcast channel (BCH) exists per provider on each GSM cell, and that channel operates at a dedicated frequency. Furthermore, channels in neighboring cells are allocated frequencies that minimize adjacent-channel interference, simplifying filter requirements (Fig. 3). Based on received signal strength indicator (RSSI) measurements throughout our 5-story building, the typical received power of a GSM BCH ranges from -65 dBm to -95 dBm, with the strongest being in the 1900-MHz band. Another larger measurement campaign also has reported similar received signal strengths [8]. Specifically, [8] reported detailed RSSI measurements of one campus building, and the received power ranged from -43 dBm to -84 dBm inside the building and from -33 dBm to -78 dBm along the exterior perimeter of the building.

B. System Operation

Fig. 4 outlines the operation of the receiver in time. The GSM standard employs Gaussian minimum-shift keying (GMSK) and other modulation schemes with pseudo-GMSK spectrums to

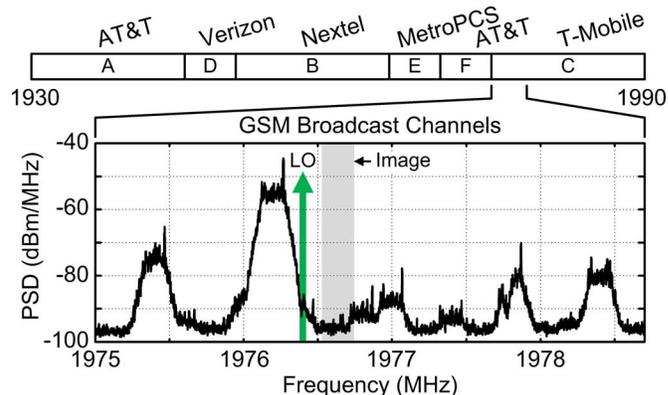


Fig. 3. GSM broadcast channels (BCHs) measured in our lab. These BCHs sit in the 1900-MHz band operated by T-Mobile, and they are spaced such that they do not interfere with each other.

modulate bursts of data in time [9]. Approximately every 46 ms, a pure sinusoidal tone is transmitted on the GSM broadcast channel. This tone burst lasts for $577 \mu\text{s}$ at an offset frequency of 67.7 kHz from the center of the channel; otherwise, data is transmitted with a spectrum occupying the entire 200 kHz channel. The bandpass filters (BPFs) in the CRX are tuned to overlapping halves of this BCH. When modulated data is transmitted by a GSM cell, the power is spread over the entire channel, passing equal signal levels through each offset BPF. During a tone burst, however, the signals captured along the two filter paths will differ. This difference in signal energies can then be detected, toggling the clock output.

C. System Architecture

The system architecture of the proposed CRX (clock-harvesting receiver) is outlined in Fig. 5. An off-chip SAW filter selects the entire 1900-MHz band, such that any GSM broadcast channel operating in the band can serve as a clock source. The input is amplified and down-converted to an intermediate frequency (IF) of 250 kHz. Channel selection is done by using different fixed local oscillator frequencies and filtering at IF.

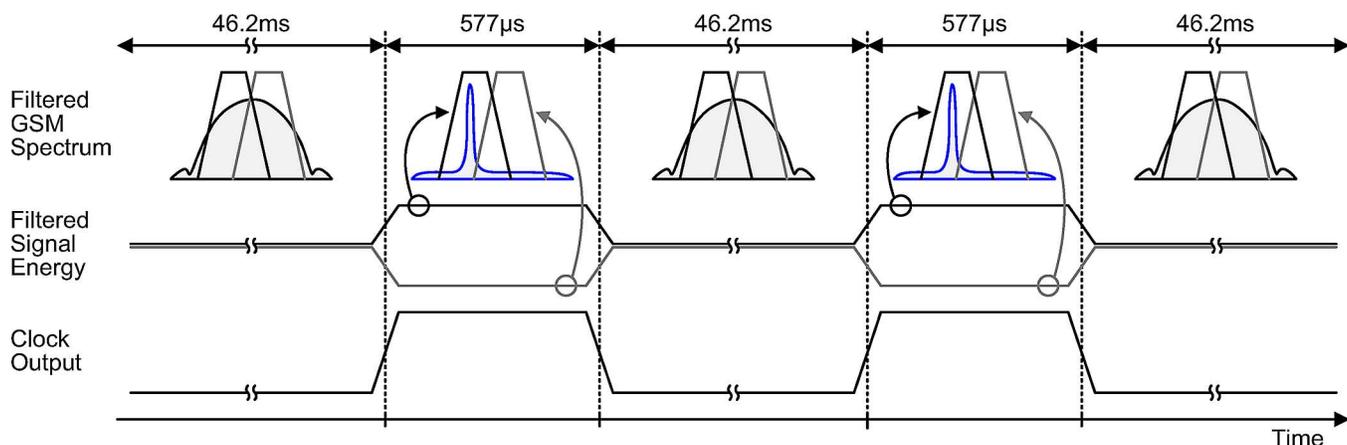


Fig. 4. Operation of a broadcast channel in time.

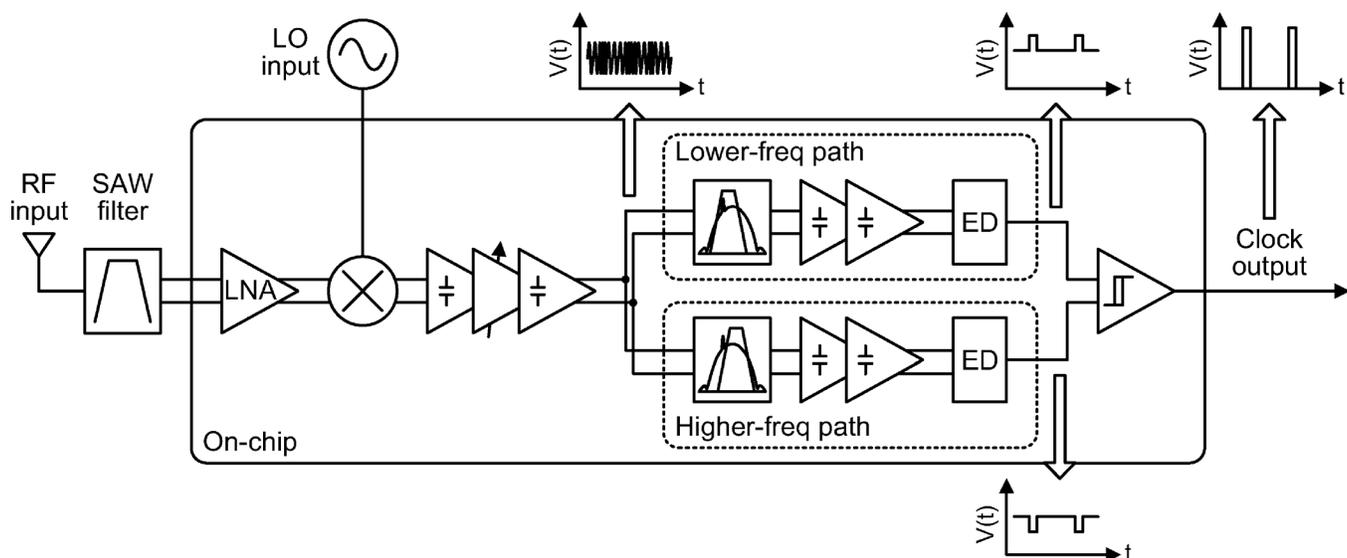


Fig. 5. System block diagram of the clock-harvesting receiver.

Fixed- and variable-gain amplifiers at IF provide gain control. Following amplification, the signal is split into two paths, each with two Gm-C BPF stages that perform sub-channel selection. Each path then amplifies and envelope detects the signal. The voltages at the output of each envelope detector (ED) are applied to a hysteretic comparator, generating a digital clock output from the harvested GSM signal.

D. Intermediate Frequency Selection

In a typical cellular network, the strongest channels in one geographic location do not sit in adjacent frequency channels in order to improve quality of service to the consumer. Based on lab measurements, the worst case frequency separation is 800 kHz between high-power channels; thus, a low IF of 250 kHz was selected (Fig. 3). The IF is low enough that the image created from down-conversion lies in a low-power adjacent channel. A low IF also lowers the quality factor requirements on the BPFs, decreasing power consumption. At the same time, the IF is high enough such that flicker noise remains low.

III. BANDPASS FILTER MODEL

In this clock-harvesting receiver, a digital clock output is generated during the intermittent tone bursts of the selected GSM broadcast channel. The tone burst is detected using filters tuned to different portions of the BCH. Therefore, optimizing the frequency response of these filters is critical to the functionality of this receiver.

Initially, we proposed the filter strategy in [10]. One filter captures the entire channel, while the other filter captures a very narrow band centered at the frequency of the tone burst. Unfortunately, the energy required to realize the narrowband filter in integrated circuits was prohibitive for a low-power system, so an alternative filter strategy was adopted. The new filter strategy uses BPFs tuned to overlapping halves of the GSM channel. They are optimized to equalize the received power during spectrally-wide data transmission and tuned to maximize received power differences during the tone bursts.

To determine the optimal characteristics of the BPFs, GMSK data was generated in MATLAB, and the bandwidth of ideal Butterworth filters was swept for several different filter orders. Then, the clock error rate (CER), defined as the number of clock

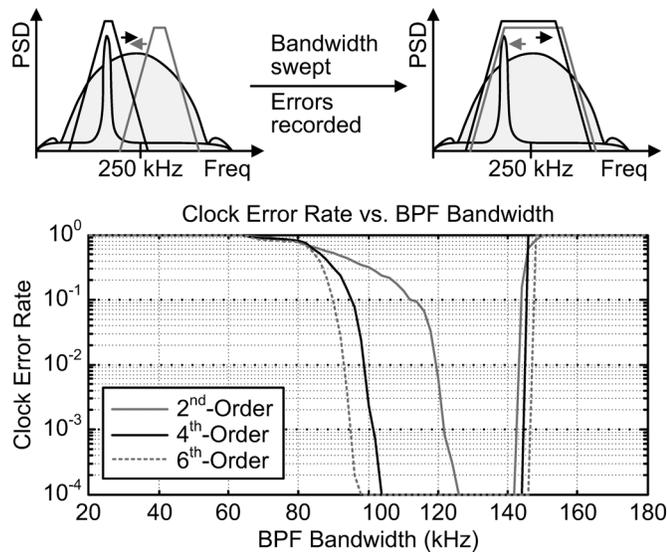


Fig. 6. Simulated clock error rate versus the bandwidth of each bandpass filter.

errors over the expected number of clock outputs, was recorded. Based on simulations shown in Fig. 6, 6th-order BPFs would allow for the largest variation in bandwidth while still having less than a 10^{-4} CER. At the same time, 6th-order filters, when realized with actual circuits, would require more power and system complexity than lower-order filters. Fourth-order BPFs, therefore, provide a good trade-off between bandwidth, power, and complexity. Simulations predict that less than 10^{-4} CER is achievable with filter bandwidths between 104 kHz and 144 kHz. The actual filter bandwidths for this receiver were then tuned to 121 kHz and 118 kHz for the lower-frequency and higher-frequency paths based on these simulations.

IV. CIRCUIT DESIGN

The system block diagram of the clock-harvesting receiver is shown in Fig. 5. The circuits in the receiver provide four primary functions: band selection and down-conversion, gain, clock detection, and sleep-power minimization.

A. RF Front-End

The RF front-end consists of a SAW filter, low-noise amplifier (LNA), and a mixer (Fig. 7). The SAW filter serves two primary functions. First, the filter serves as a balun for single-to-differential conversion from the antenna to the differential inputs of the receiver. Second, the filter serves as a bandpass filter for the downlink side of the 1900-MHz band (also called the PCS band). The GSM standard separates the uplink side of the 1900-MHz band for mobile-phone-to-base-station communication from the downlink side of the band for base-station-to-mobile-phone communication. To prevent possible saturation of the RF front-end from the uplink side of the 1900-MHz band, the uplink portion is rejected by the filter. The filter is designed to match to $50\ \Omega$ single-ended at the input and $100\ \Omega$ differential at the output.

To reduce active power in the receiver, the system has only one RF gain stage before mixing down to a low IF. The RF inputs are AC-coupled on-chip directly to an un-matched fully-differential low-noise amplifier with inductive loading

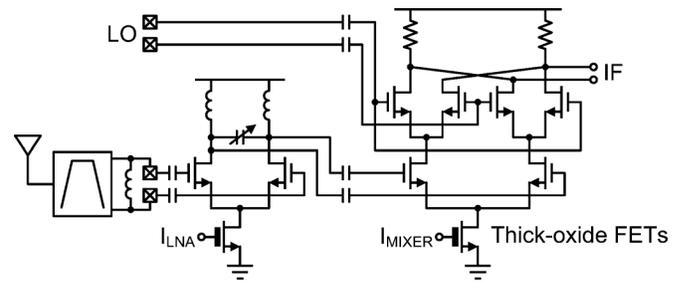


Fig. 7. RF front-end, including SAW filter, LNA, and mixer.

(Fig. 7). The inductors are sized to maximize their impedance in the band-of-interest, and a varactor was added in order to tune center frequency. The varactor is sized to account for process variation while still passing every channel in the 1900-MHz band. The LNA is fully-differential in order to provide common-mode rejection and simplify biasing of the input devices. Current biasing is accomplished with a thick-oxide FET which also provides lower sleep-mode leakage current. While a single-ended implementation would require half the power in active mode for equal gain, higher active power due to the additional voltage headroom requirement was traded for the ability to reduce sleep-mode power with a thick-oxide tail device.

The LNA output is AC-coupled to a double-balanced Gilbert-cell mixer (Fig. 7). A Gilbert mixer provides good common-mode rejection and also has less RF and LO feedthrough than a single-ended implementation. The remaining RF and LO feedthrough is attenuated by the IF gain stages. Headroom is a challenge, but the problem is mitigated with the use of low threshold voltage devices for the RF and LO inputs and moderately sized load resistors. As with the LNA, the bias current of the fully-differential mixer can be shut-off in sleep mode with the use of a thick-oxide FET.

The local oscillator is generated off-chip and is used to select the desired GSM broadcast channel. The bandpass filters at IF have a measured tuning range that allows for up to 161 ppm in frequency drift from the LO across temperature or process while still maintaining proper receiver functionality. In addition, the broadcast channels at a given geographic location can be measured with either a spectrum analyzer or a mobile phone in field test mode. A desirable BCH then can be determined, and a fixed LO can be used with the CRX. Based on these specifications, a low-power local oscillator should be feasible. For example, FBAR-based fixed-frequency LOs consuming less than $100\ \mu\text{W}$ have been reported [5], [6], which could be used to target a specific GSM broadcast channel.

A fixed LO solution, however, does assume the frequency allocation plan of the local GSM broadcast channels remains unchanged during the life of the WSN, and over many months of design and testing, the targeted BCH in our geographic location did not change, so we believe this assumption has significant merit for many WSNs.

B. Baseband Gain Stages

Once the signal is at IF, amplification is provided by four differential fixed-gain amplifiers (FGAs) and one vari-

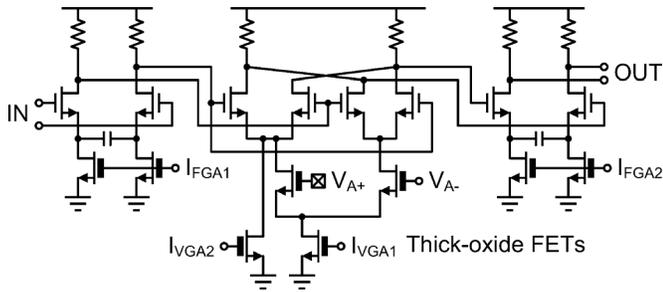


Fig. 8. Baseband amplifiers, including two fixed-gain amplifiers and one VGA.

able-gain amplifier (VGA). Each fixed-gain amplifier consists of low-threshold voltage input FETs, resistive loads, and split-source with capacitive-coupling (Fig. 8) [2], [11]. To reduce noise, the first FGA after the mixer is sized differently from later gain stages. The first gain stage has a simulated bias current of $3 \mu\text{A}$ and load resistance of $167 \text{ k}\Omega$. Later gain stages, on the other hand, have a simulated bias current of $1 \mu\text{A}$ and load resistance of $500 \text{ k}\Omega$. The gain stages are biased in weak inversion, which provides good gain efficiency (g_m/I_D) and linearity. The simulated gain for all stages is 13 dB .

The split-source capacitor is placed between the input source terminals of the FGA. The capacitor adds a zero to the transfer function of the amplifier, creating a bandpass response to the overall gain stage. Near DC, the capacitor looks like a large impedance, which strongly degenerates the amplifier resulting in no gain and eliminating accumulated offset voltages. Without accumulated offset voltages, common-mode feedback becomes unnecessary.

Because the intermediate frequency is only 250 kHz , resistive loading provides ample bandwidth, while also making DC-coupling possible. Precise sub-channel filtering is performed in the Gm-C bandpass filters further down the signal path, so the pass-band of these FGAs extend below and above the frequencies of interest. As a result, the lower-cutoff frequencies are set to 25 kHz for the first gain stage and 27 kHz for the later gain stages based on simulations. The upper-cutoff frequencies are set to 11 MHz and 17 MHz , respectively.

The topology of the variable-gain amplifier is very similar to that of a double-balanced Gilbert mixer or an analog multiplexer [12]; however, this topology adds a current source for one of the input differential pairs (Fig. 8) and is based on an unfolded version of [12]. Gain is varied by changing the voltage difference between V_{A+} and V_{A-} . Only one of these voltages (V_{A+}) is set off-chip, while the other is fixed on-chip. High-threshold NFETs were used for the gain inputs (V_{A+} and V_{A-}) in order to provide a larger input tuning range, so that a fixed off-chip voltage tuning can provide stable on-chip gain.

To understand the operation of this VGA, it is easiest to first ignore the second current source (I_{VGA2}). In this case and when V_{A+} and V_{A-} are equal, equal currents are steered through each input differential pair, producing equal gain. Each differential pair, however, shares a single pair of resistive loads with inputs that are 180° out-of-phase. As a result, the voltages cancel, and the gain is 0 V/V ($-\infty \text{ dB}$). Therefore, as V_{A+} ramps from rail-to-rail while V_{A-} is held constant, the gain decreases

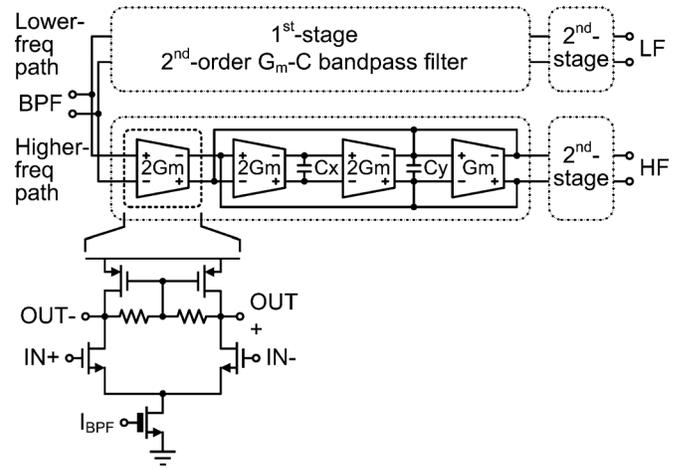


Fig. 9. Two-stage bandpass filters for the lower-frequency and higher-frequency paths.

until V_{A+} and V_{A-} are equal, then increases again—a non-monotonic response. A non-monotonic response makes external tuning needlessly difficult. To address this, a second tail current (I_{VGA2}) is added. The second current source ensures that the left differential pair always has more current than the right pair, so that the gain increases monotonically with V_{A+} . For this VGA, the first current source is set to $1 \mu\text{A}$ in simulation, and the second current source is set slightly larger.

C. Filtering and Clock Extraction

To detect the clock embedded in the GSM standard, the amplified IF signal is split into two sub-channels: a lower-frequency path and a higher-frequency path. Each signal path has a 2-stage Gm-C bandpass filter tuned to overlapping halves of a GSM broadcast channel.

Each Gm-C stage consists of a differential 2nd-order filter with unit transconductors for better matching. The unit transconductors consist of differential pairs with PMOS load and resistive CMFB for self-biasing (Fig. 9). Each unit consumes only 200 nA . Very large resistance is achieved by using reverse-biased FETs. In addition, one self-biasing network is shared by all unit transconductors connected to the same differential signals. In other words, two self-biasing networks exist per Gm-C bandpass filter stage; one network across C_x and the other across C_y . The capacitors in each path and for each stage are sized to provide a Butterworth response, and unit MIM capacitors are used for better matching. The magnitude response of each BPF is tuned to equalize the received power through overlapping halves of the GSM channel during data bursts and to maximize received power differences during tone bursts.

The bandwidths of the BPFs along the lower- and higher-frequency paths are 121 kHz and 118 kHz , respectively. They are optimally determined by system simulations to minimize the clock error rate (CER), defined as the number of clock errors over the expected number of clock outputs (Fig. 6) [10]. Additionally, the use of two wideband filters decreases quality factor requirements over the detection method we originally proposed in [10], reducing the power required to filter the GSM channel.

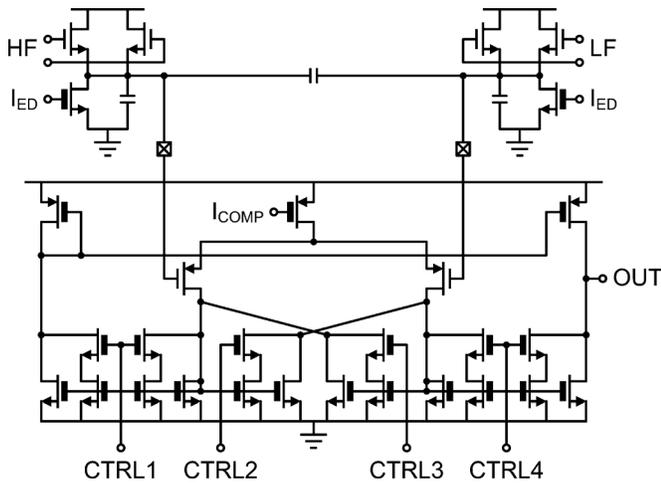


Fig. 10. Envelope detectors and continuous-time comparator.

The BPFs produce nominal gain in order to reduce active power. Each Gm-C BPF stage consists of seven unit transconductors. At 200 nA/unit-Gm the transconductors do not generate significant gain, but each stage still draws more current than a single FGA. Thus, additional gain was generated after filtering using two FGAs for each path.

The signal powers in the lower- and higher-frequency paths are converted to DC through two passive envelope detectors (EDs). The EDs have differential inputs and single-ended output, and each ED draws 100 nA. The 21-Hz harvested clock has pulses with 577 μ s duration. Therefore, large 100 pF capacitors are connected to ground in order to decrease bandwidth and slow the response at the output of each ED. To eliminate instantaneous differences at the output of the EDs, the two paths are capacitively-coupled together with a 50 pF capacitor, so that high frequency signal components are shorted between the outputs.

The received signal powers through the lower-frequency and higher-frequency paths are compared using a 2-stage continuous-time comparator with programmable hysteresis (Fig. 10). The ED outputs are directly coupled to the input PFETs of the comparator. The load of the first stage of the comparator creates hysteresis, which prevents spurious switching of the output. The load consists of a combination of cross-coupled and diode-connected NFETs. The relative drive strength of the cross-coupled and diode-connected NFETs sets the hysteresis levels. Additional parallel NFETs can be digitally-enabled with four NMOS switches in order to adjust the initial hysteresis levels either up or down. The second stage provides differential-to-single-ended conversion as well as additional gain. Finally, the harvested 21-Hz clock output is sent through a buffer to be driven off-chip.

D. Sleep-Power Minimization

In heavily duty-cycled operation, sleep-mode energy dominates active-mode energy; however, no recently reported low-power radios address sleep-mode power in their designs. In this CRX, thick-oxide tail devices were added to every stage in the receiver's signal path and its bias generation in order to minimize sleep-mode leakage currents (Figs. 7–10). Using

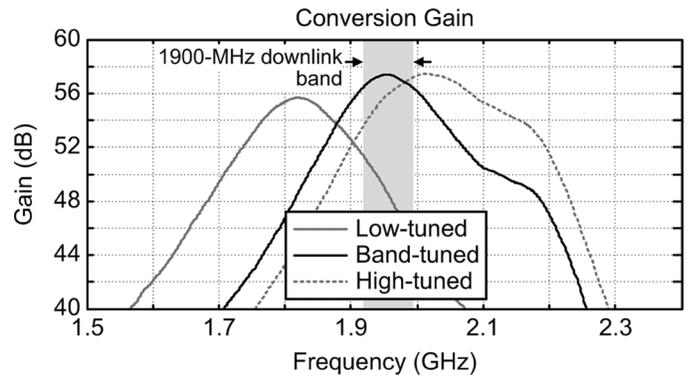


Fig. 11. Conversion gain for different tunings of the varactor.

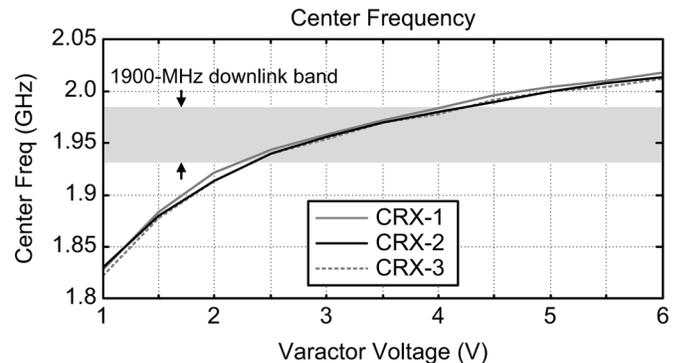


Fig. 12. Center frequency across varactor voltage for multiple die.

thick-oxide tail devices, however, increases active-mode energy due to the larger headroom requirements for the high-threshold voltage devices. In this case, 300 mV of additional headroom was used for the tail devices. Sizing of the thick-oxide devices was done to maximize the ratio between active-mode and sleep-mode current.

V. MEASUREMENT RESULTS

The clock-harvesting receiver was fabricated in a 0.13 μ m CMOS process with MIM capacitors. The entire receiver operates from a single 1 V supply. The conversion gain of the CRX is shown in Fig. 11 at three differently tuned varactor voltages in the LNA. The peak conversion gain measured at sensitivity is 57 dB, and gain-control is achieved by tuning the VGA and the tail bias currents of each stage. The measured bandwidth of the LNA is 140 MHz.

The center frequency of the receiver was measured across varactor voltage for three die (Fig. 12). The center frequency plotted corresponds to the frequency at which conversion gain peaked for each varactor voltage. The LNA for each die can be tuned with the varactor over a worst-case frequency range of 1.83 to 2.01 GHz. Therefore, all three die can be tuned over the entire downlink side of the 1900-MHz band, enabling the selection of any broadcast channel in the US.

The BPFs for the lower- and higher-frequency paths are critical to the overall functionality of the CRX. Their magnitude response is measured at the output of the envelope detectors (Fig. 13). The bandwidths of the BPFs along the lower- and higher-frequency paths are 121 kHz and 118 kHz, respectively, based

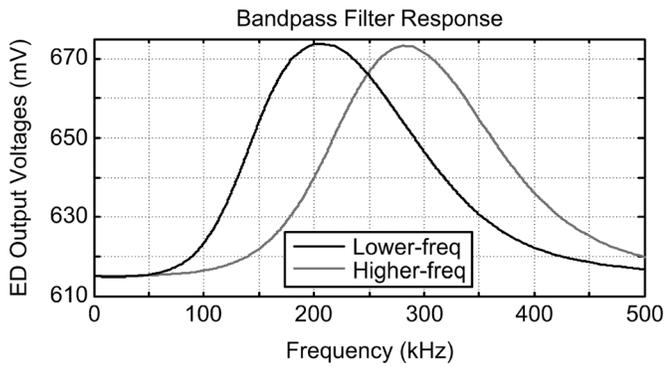


Fig. 13. Magnitude response of the bandpass filters.

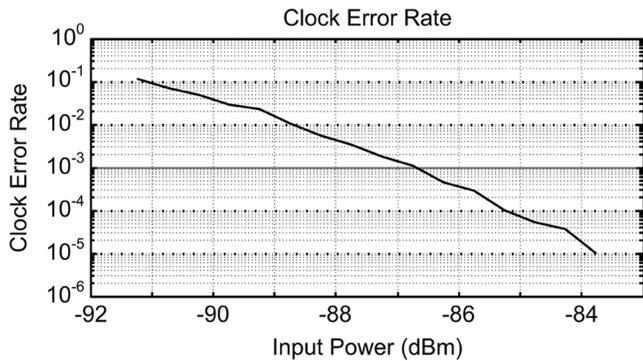


Fig. 14. Clock error rate vs. input power.

on system simulations to minimize the clock error rate (Fig. 6). Additionally, both the bandwidth and center frequency of each filter is tunable in order to change the intermediate frequency if necessary.

The measured CER (clock error rate) versus input power is shown in Fig. 14. At a CER of 10⁻³, the peak sensitivity is -87 dBm with a total power consumption of 126 μ W, of which the front-end consumes 98 μ W and the baseband consumes 28 μ W. At a reduced sensitivity of -60 dBm while maintaining 10⁻³ CER, the total power consumption of the receiver can be reduced to 67 μ W. Proper operation was verified at input powers up to -5 dBm. In sleep mode, the leakage power of the system is 81 pW.

The path delay and clock jitter were measured for two different die (Fig. 15). A pseudo-GSM broadcast channel was generated on an arbitrary waveform generator (AWG), then up-converted and sent into the two clock-harvesting receivers. At the start of each tone burst, a synchronization marker was generated by the AWG. Delay and jitter were then recorded. From this setup, the average delay in clock output is 109 μ s for CRX-1, and 104 μ s for CRX-2, which is predominately due to the slow response of the EDs. The measured jitter at peak sensitivity is 57 μ s. At higher signal powers, the jitter reduces to approximately 7 μ s worst case. The average chip-to-chip time difference is 5.1 μ s with a jitter of 7.6 μ s, which suggests that network synchronization can be achieved with better than 50 μ s accuracy ($6\sigma + \mu$). The start-up time from sleep mode to active mode is roughly 500 μ s, limited by slewing at the ED outputs.

The signal-to-interference ratio (SIR) was measured for interfering GSM signals in neighboring channels (Fig. 16). A broad-

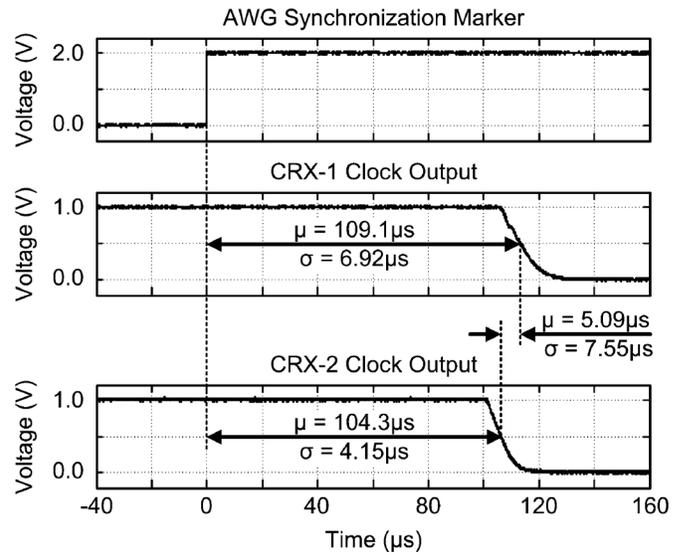


Fig. 15. Delay and jitter measurements of two clock-harvesting receivers.

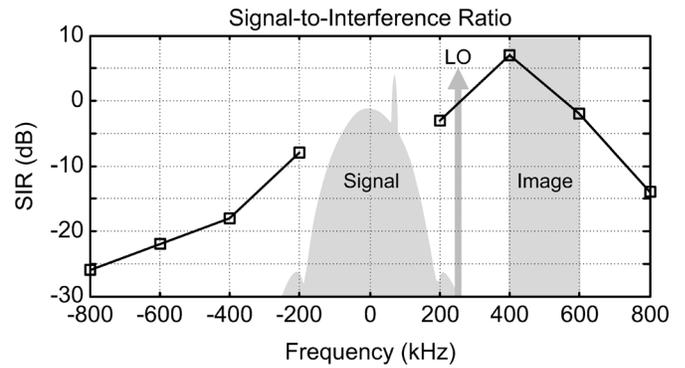


Fig. 16. Signal-to-interference ratio for neighboring broadcast channels.

cast channel was generated at a fixed frequency while a second interfering channel was generated at a frequency up to 800 kHz above or below the BCH frequency. The SIR was varied until the CER reached 10⁻³. Based on measured BCH allocations in the lab, interfering BCHs reside at least 800 kHz away from the target BCH (Fig. 3). The worst case SIR is -14 dB at this frequency offset. Thus, by selecting the highest power BCH in a given geographic location, the CRX always can be harvested, assuming a typical GSM channel allocation policy. Even with an atypical allocation policy, the measured SIR is only 7 dB at the image. Thus, an image has a negligible effect on performance in most channel environments so long as the desired BCH is >7 dB above the image, which will occur away from the cell boundary. Finally, the SIR results similarly indicate that the IF bandwidth can be safely tuned to adjust for frequency variation in the LO for nearly all channel environments.

The core circuit area occupies approximately 0.99 mm² (Fig. 17). The area is dominated by the two inductors of the differential LNA and the capacitors for the EDs. The capacitors for the FGAs also occupy a noticeable amount of area along with the unit capacitor array created for the BPFs.

To illustrate how a WSN could be synchronized using CRXs, two clocks were harvested simultaneously from the 1976.2 MHz GSM broadcast channel of a local tower (T-Mobile) using two

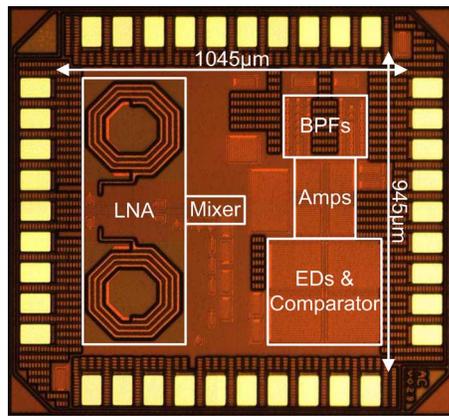


Fig. 17. Die photo.

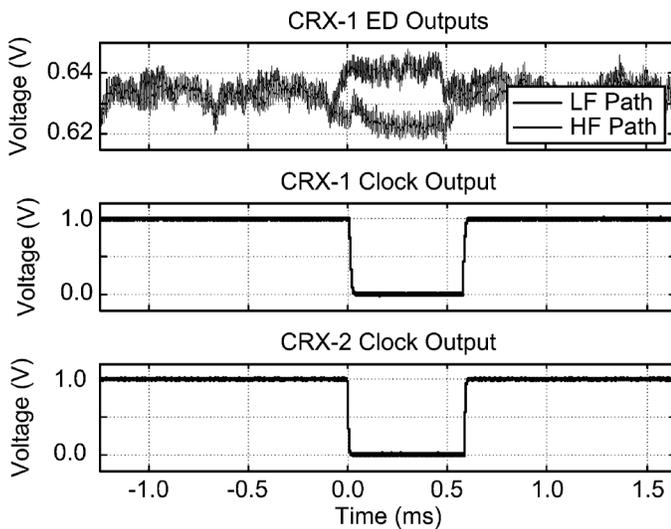


Fig. 18. Simultaneously harvested-clocks of two CRXs from a local GSM broadcast channel.

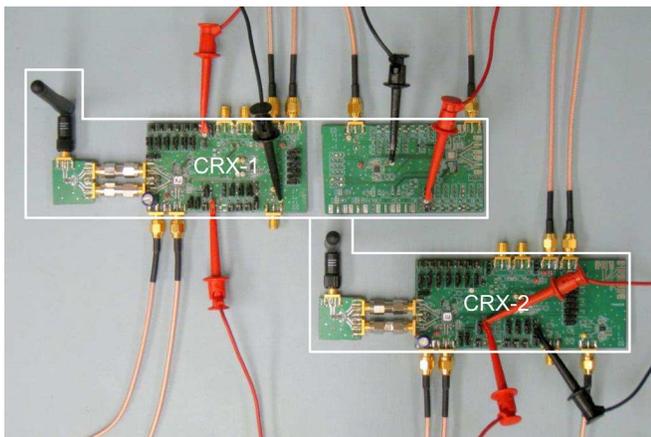


Fig. 19. Setup of two CRX debug boards receiving a real GSM signal in our lab.

CRXs placed 10 cm apart on a table. The resulting clock outputs are shown in Fig. 18. The envelope detected outputs for one CRX are shown in the figure as well. During wideband bursts,

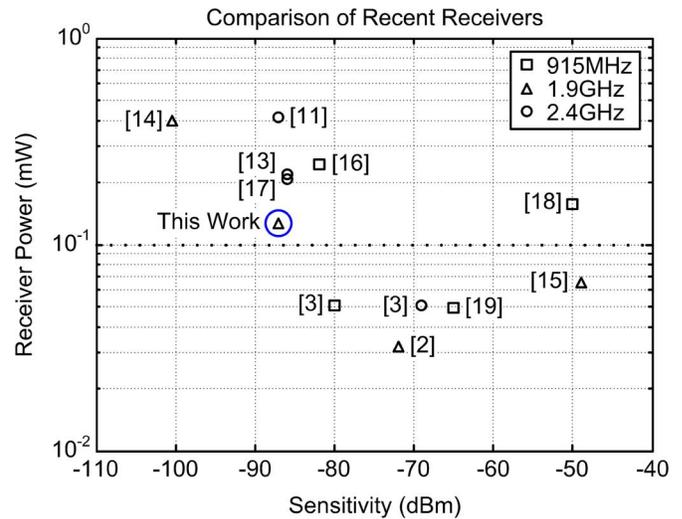


Fig. 20. Comparison of power consumption vs. sensitivity of recent wake-up receivers. The active power for other works excludes the local oscillator when possible or applicable.

TABLE I
DETAILED PERFORMANCE SUMMARY AND COMPARISON

	This Work	[2]	[3]	[11]
Process	0.13µm	90nm	90nm	65nm
RX Type	Clock-harvest	Wake-up	Wake-up	Wake-up
V _{DD}	1.0V	0.5V	0.5V	1.2V
Area	0.99mm ²	0.1mm ²	0.36mm ²	0.2mm ²
Sensitivity (@ 10 ⁻³ BER)	-87dBm	-72dBm	-80dBm	-87dBm
P _{Active} P _{Sleep}	126µW 81pW	52µW	51µW	415µW
P _{Front-End}	98µW	56pW	8µW	199µW
P _{Baseband}	28µW	25pW	24µW	51µW
Jitter (@ Sensitivity)	57µs	N/A	N/A	N/A
Gain _{Conversion}	57dB	Unknown	Unknown	61dB
F _{Center}	1.9GHz	2GHz	915MHz, 2.4GHz	2.4GHz
t _{Start-Up}	500µs	Unknown	Unknown	Unknown
Required LO Accuracy	161ppm	10 ⁵ ppm	N/A	5x10 ³ ppm

the envelope-detected outputs are approximately equal as expected. During the tone burst however, the ED outputs differ, toggling the comparator output of both receivers. The photo of the test setup is shown in Fig. 19. Both CRXs extracted the real GSM clocks in our lab using small monopole antennas.

This clock-harvesting receiver is compared with several recent wake-up receivers and low-power communication receivers for WSNs, and the active power consumption is plotted versus sensitivity (Fig. 20). The active power for other works excludes power for the local oscillator when possible or applicable to create a more fair comparison with this work. A detailed performance summary is provided in Table I along with a comparison to a few select WRXs.

VI. CONCLUSION

A new type of wake-up receiver, called the clock-harvesting receiver (CRX), is presented that is capable of extracting a 21-Hz clock embedded within the GSM standard for the wake-up of a wireless sensor network. By harvesting the clock from a pre-existing and pervasive source, the WSN does not have to generate it within the network. In addition, the CRX can be heavily duty-cycled for use in a tiered synchronization strategy to greatly reduce synchronization energy. Measurements show that the receiver achieves -87 dBm sensitivity while consuming only $126 \mu\text{W}$. In sleep-mode, the power consumption is 81 pW . The functionality of two clock-harvesting receivers was verified by extracting a clock from the broadcast channel of a local cell tower.

ACKNOWLEDGMENT

The authors would like to thank C² Systems for providing GSM signal strength data of our building.

REFERENCES

- [1] B. H. Calhoun *et al.*, "System design principles combining sub-threshold circuits and architectures with energy scavenging mechanisms," in *IEEE Int. Symp. Circuits and Systems (ISCAS 2010)*, Jun. 2010, pp. 269–272.
- [2] N. Pletcher, S. Gambini, and J. M. Rabaey, "A $52 \mu\text{W}$ wake-up receiver with -72 dBm sensitivity using an uncertain-IF architecture," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 269–280, Jan. 2009.
- [3] X. Huang *et al.*, "A 2.4 GHz/915 MHz $51 \mu\text{W}$ wake-up receiver with offset and noise suppression," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 222–223.
- [4] Y.-S. Lin, D. Sylvester, and D. Blaauw, "A 150 pW program-and-hold timer for ultra-low power sensor platforms," in *IEEE ISSCC Dig. Tech. Papers*, 2009, pp. 326–327.
- [5] Y. H. Chee, A. M. Niknejad, and J. Rabaey, "A sub- $100 \mu\text{W}$ 1.9-GHz CMOS oscillator using FBAR resonator," in *IEEE RFIC Symp.*, Jun. 2005, pp. 123–126.
- [6] A. Nelson *et al.*, "A $22 \mu\text{W}$, 2.0 GHz FBAR oscillator," in *IEEE RFIC Symp.*, Jun. 2011, pp. 1–4.
- [7] "GSM world coverage 2009," GSM World, 2009-A ed., GSM Association, Jan. 2009 [Online]. Available: http://www.coveragemaps.com/gsmposter_world.htm, [Accessed: Sep. 10, 2009]
- [8] J. Zhu, "Indoor/outdoor location cellular handsets based on received signal strength," Ph.D. dissertation, Sch. Electr. Comput. Eng., Georgia Inst. Tech., Atlanta, GA, USA, 2006.
- [9] *Global System for Mobile Communications*, European Telecommunications Standards Institute, Feb. 2009, Tech. Spec., 145 Series, v. 8.0.0.0, Release 8.
- [10] J. K. Brown and D. D. Wentzloff, "Harvesting a clock from a GSM signal for the wake-up of a wireless sensor network," in *IEEE Int. Symp. Circuits and Systems (ISCAS 2010)*, Jun. 2010, pp. 1500–1503.
- [11] S. Drago *et al.*, "A 2.4 GHz 830 pJ/bit duty-cycled wake-up receiver with -82 dBm sensitivity for crystal-less wireless sensor nodes," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 224–225.

- [12] C.-H. Wu, C.-S. Liu, and S.-L. Liu, "A 2 GHz CMOS variable-gain amplifier with 50 dB linear-in-magnitude controlled gain range for 10 GBase-LX4 ethernet," in *IEEE ISSCC Dig. Tech. Papers*, 2004, pp. 484–485, 541.
- [13] J. Ayers, K. Mayaram, and T. S. Fiez, "An ultralow-power receiver for wireless sensor networks," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1759–1769, Aug. 2010.
- [14] B. Otis, Y. H. Chee, and J. Rabaey, "A $400 \mu\text{W}$ -RX, 1.6 mW -TX super-regenerative transceiver for wireless sensor networks," in *IEEE ISSCC Dig. Tech. Papers*, 2005, pp. 396–606.
- [15] N. Pletcher, S. Gambini, and J. Rabaey, "A $65 \mu\text{W}$ 1.9 GHz RF to digital baseband wakeup receiver for wireless sensor nodes," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2007, pp. 539–542.
- [16] J. Ayers, K. Mayaram, and T. S. Fiez, "A 0.4 nJ/b 900 MHz CMOS BFSK super-regenerative receiver," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2008, pp. 591–594.
- [17] J. Ayers, N. Panitantom, K. Mayaram, and T. S. Fiez, "A 2.4 GHz wireless transceiver with 0.95 nJ/b link energy for multi-hop battery-free wireless sensor networks," in *IEEE VLSI Symp. Dig.*, 2010, pp. 29–30.
- [18] Y. Han *et al.*, "An ultra low power BPSK receiver and demodulator based on injection-locked oscillators," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 5, pp. 1339–1349, 2011.
- [19] M. Lont *et al.*, "Ultra-low power FSK wake-up receiver front-end for body area networks," in *IEEE RFIC Symp. Dig.*, 2011.



Jonathan K. Brown received the B.S.E. and M.S.E. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2007 and 2008, respectively, before completing the Ph.D. degree at the University of Michigan, Ann Arbor, in 2012.

He now works at Cavium, Marlborough, MA, USA, doing mixed-signal circuit design for high-speed wireline communication.

Dr. Brown was a recipient of a 2011 DAC/ISSCC Student Design Contest Award.



David D. Wentzloff received the B.S.E. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 1999, and the S.M. and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2002 and 2007, respectively.

In the summer of 2004, he worked in the Portland Technology Development group at Intel, Hillsboro, OR, USA. Since August 2007, he has been with the University of Michigan, Ann Arbor, where he is currently an Assistant Professor of Electrical Engineering and Computer Science.

Dr. Wentzloff is the recipient of the 2002 MIT Masterworks Award, 2004 Analog Devices Distinguished Scholar Award, 2009 DARPA Young Faculty Award, 2009–2010 Eta Kappa Nu Professor of the Year Award, 2011 DAC/ISSCC Student Design Contest Award, 2012 IEEE Subthreshold Microelectronics Conference Best Paper Award, and the 2012 NSF CAREER Award. He has served on the technical program committee for ICUWB 2008–2010, ISLPED 2011–2012 and RFIC 2013, and as a guest editor for the *IEEE T-MTT*, the *IEEE Communications Magazine*, and the *Elsevier Journal of Signal Processing: Image Communication*. He is a member of IEEE, IEEE Circuits and Systems Society, IEEE Microwave Theory and Techniques Society, IEEE Solid-State Circuits Society, and Tau Beta Pi.